Fermi National Accelerator Laboratory

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Engineering Note

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Project: D0 Tracking Electronics
Doc. No: U000611A

Subject: SVX Sequencer Test Procedure

1) Visual inspection
- Are the correct chips installed properly?
- Any obvious soldering problems.
- Ohm meter: 55 ohms +5V to GND, kOhms –5.2V to GND.

2) Install board into crate, attach fibers, and turn on SVX Power and crate power. Plug in Altera Byteblaster and program EPLDs on board using MaxPlusII software, Programmer.
3) Initialize VRB and VRBC.
4) Initialize Sequencer by executing 1553 commands as shown in Appendix A. Make sure the readbacks are correct.
5) Download SVX chips as in spreadsheet.
6) Do one Cal Pulse cycle and for each of the eight SVX strings, check the following:
- Is Sequencer ID correct
- Is Sequencer Status byte correct
- Are chip Ids correct
- Do channel Ids increment by one
- Is data pedestal within +/- 10 counts
- Is the trailer C0C0 at the end of the data for each string

7) Set the Cal Voltage parameter to various values and check that the value read out in the data is within limits. Suggested Cal Voltage values: 00, 01, 02, 04, 08, 10, 20, 40, 80, FF. An alternative is to probe the Vcal pin going to the HDI. I have nominal values for these measurements.
8) With a scope probe on the SVX clock line, check crossing pulse width while in Acquire mode. Nominal values exist for various values of this parameter.
9) Check readout at various pipelines 00, 01, 02, 04, 08, 10, 1F, by setting the Cal Pipe parameter to match the setting of the SVX pipeline depth for one chip. Then make sure the Cal pulses exist in every case.
10) Set Sequencer ID to 00, 01, 02, 04, 08, 10, 20, 40, 80, FF and check that the readout header matches.
11) Check the eight possible settings of CSR1 bits 9, 10, 11 (Diagnostic Port Select) by reading Subaddress 12 for each setting. A more sophisticated test would be to run the Logic Analyzer feature for each setting.
12) Test the Logic analyzer feature using the Cal and Readout trigger options.
13) Remove NRZ and check CSR1 bits 3 and 4.

14) Try software reset, bit 7 of CSR1.
15) Check Subaddresses E and F for testing fiber data path via 1553 fake data.
16) Check that Subaddresses E and F properly set the FIFO AF offsets. This requires hooking up a logic analyzer to the FIFOs.
17) Check that the Finisar Serial Number reads out and temp is about 32 hex. (48C)
18) With a scope check 1553 output by probing J1C2, J1C3.
19) Using a 40MHz crystal, check slow readout for each half of board.